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ULTRA-THIN BODY SUPER-STEEP RETROGRADE WELL (SSRW) FET DEVICES

Abstract

A method of manufacture of a Super Steep Retrograde Well Field Effect Transistor device starts with an SOI layer formed on a substrate, e.g. a buried oxide layer. Thin the SOI layer to form an ultra-thin SOI layer. Form an isolation trench separating the SOI layer into N and P ground plane regions. Dope the N and P ground plane regions formed from the SOI layer with high levels of N-type and P- type dopant. Form semiconductor channel regions above the N and P ground plane regions. Form FET source and drain regions and gate electrode stacks above the channel regions. Optionally form a diffusion retarding layer between the SOI ground plane regions and the channel regions.